

**DIGITAL ELECTRONICS**

**DEE 4544**

**EXPERIMENT 1**

**STUDENT NAME:**

**STUDENT ID:**

**PROGRAMME:**

**SEMESTER:**



**FACULTY OF ENGINEERING**

**EXPERIMENT 1 (CO4, PO7):**

**Evaluate combinational logic circuits using Multisim Live. (C4, PLO7).**

* 1. **Objectives**

To verify truth table of logic gates (NOT, AND and OR gates).

**2.0 Software**

Multisim Live

**3.0 Theory**

The inverter (NOT circuit) performs the operation called inversion or complementation. The NOT operation changes one logic level to the opposite logical level. When the input is low, the output is high. When the input is high, the output is low.

An AND gate can have two or more inputs and performs what is known as multiplication.

The output of AND gate is high when all inputs are high otherwise all outputs are low.

OR gate can have two or more inputs and performs what is known as logical addition.

The output of OR gate is Low when all inputs are low, otherwise all outputs are high.

**4.0 Problem Statement**

1. Verify the truth table of NOT gate.

A red and white stripes

Description automatically generatedA black triangle with a circle and a dot

Description automatically generated

1. Verify the truth table of AND gate.

A table with numbers and symbols

Description automatically generated A black line drawing of a wire

Description automatically generated

1. Verify the truth table of OR gate.

A table with numbers and symbols

Description automatically generated A white line with a curved arrow

Description automatically generated with medium confidence

**5.0 Results**

(Show the screenshot of the circuit simulation, and the output graph)

**6.0 Observations** (note: discuss your observation from the experimental results)

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**7.0 Conclusion**

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**COURSE: DIGITAL ELECTRONICS (BEE 2123)**

**LAB EXPERIMENT 1 (C4, PO7): Evaluate combinational logic circuits using Multisim Live.**

**Rubric for the lab report**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Criteria | Excellent  5 | Very Good  4 | Good  3 | Poor  2 | Very Poor  1 |
| Ability to construct the basic logic circuit | Fully able to construct the basic logic circuit | Reasonably able to construct the basic logic circuit | Not quite able to construct the basic logic circuit | Poor ability to construct the basic logic circuit | Very poor ability to construct the basic logic circuit |
| Ability to verify the truth table of logic gates | Fully able to verify the truth table of logic gates | Reasonably able to verify the truth table of logic gates | Not quite able to verify the truth table of logic gates | Poor ability to  verify the truth table of logic gates | Very poor ability to verify the truth table of logic gates |